WHAT IS CLAIMED IS:

1. A method for enhancing the efficiency of the performance of a linear transformation represented by an *rxn* matrix of at least one n-dimensional input vector above the real or complex or a finite field comprising:

storing in memory a ratio between each omitted row and each selected row;

omitting zero columns of said matrix and the corresponding scalar components of the input vector;

normalizing each column of said matrix;

generating a modified vector from groups of equal columns in the normalized matrix;

generating a modified matrix; and

obtaining the output vector.

2. The method of Claim 1, further comprising splitting the transformation matrix into several sub-matrices and obtaining the output vector by unifying the output vectors resulting from the products of each sub-matrix.

3. The method of Claim 2, wherein the modified matrix encompasses a subset of rows of said transformation matrix.

4. The method of Claim 3, further comprising splitting the input vector into several sub-vectors such that each sub-vector corresponds to a sub-matrix and wherein the output vector is obtained by adding the output vectors resulting from the products of each sub-matrix.

5. The method of Claim 1, further comprising splitting a modified matrix into several sub-matrix, wherein an output vector is obtained by adding the output vectors resulting from the products of each sub-matrix, by the respective sub-vector.

6. The method of Claim 1, further comprising normalizing each column of said matrix by multiplying the column by the inverse of a lead element.

7. The method of Claim 1, wherein the output vector is a product of the matrix and the input vector.

8. The method of Claim 1, further comprising identifying groups of equal columns in the normalized matrix and attaching a unique location to each identified group.

9. An apparatus for performing a linear transformation, comprising:

first and second inputs which receive input data and predetermined data;

transformation circuitry which acts on the input data and predetermined data;

control and address generation circuitry, connected to a first memory, which generates corresponding addresses for accessing cells of said memory, and for controlling the selection between a data receiving mode, in which data is received via said first input, and a data processing mode, in which the arrival of incoming data via said first input is blocked; and

counter circuitry for controlling the timing of the operations the apparatus.

10. The apparatus of claim 9, wherein the transformation circuitry multiplies each element of the input data by a corresponding element of the transformation data.

11. The apparatus of claim 10, wherein the transformation circuitry comprises a memory which stores the result of the multiplication.

12. The apparatus of claim 9, wherein the transformation circuitry comprises summation and accumulation circuitry.

13. The apparatus of claim 9, further comprising a multiplexer circuitry which selects between the data receiving mode and the data processing mode.

14. The apparatus of Claim 9, wherein the control and address generation circuitry comprises:

a second memory which stores pre-programmed processing and control data and;

a comparator circuitry which switches between the data receiving mode and the data processing mode.

15. The apparatus of Claim 14, wherein the control and address generation circuitry further comprises:

a first set of multiplexers, each of which having at least one direct input for receiving transformation data, and another input, into which said transformation data is fed via a corresponding inverter, said first set being controlled to transfer transformation data or, inverted transformation data, by a predetermined value provided by said transformation data;

a second set of multiplexers, each of which having at least one input connected to the output of a corresponding multiplexer selected from said first set of multiplexers, and another input, connected to said second memory, said second set being controlled by said comparator circuitry to provide a first address to the first memory by transferring the output of each multiplexer from said first set to the output of its

corresponding multiplexer from said second set or, to provide at least a portion of the second address to the first memory by transferring data stored in said second memory; and

a multiplexer, operating in combination with said second set of multiplexers in said data processing mode, having an unconnected input and an input connected to said second memory and controlled by said comparator circuitry, thereby providing the remaining portion of said second address.